AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Claims 1-19 (Canceled)

20.   (Previously presented)   An apparatus comprising:

a transmitter that transmits data with a predetermined size to a receiver via a serial transmission, the data having an identifier number and an error check signal; and

a buffer that is coupled to the transmitter and stores transmitted data, and wherein the transmitter repeatedly transmits the transmitted data stored in the buffer, and terminates transmitting the transmitted data if an affirmative acknowledgement indicates that the identifier number of data that is received by the receiver is returned from the receiver.

21.   (Previously presented)   The apparatus according to claim 20, wherein the transmitter purges the transmitted data stored in the buffer if the affirmative acknowledgement indicates that the transmitted data is received from the receiver.

22.   (Previously presented)   The apparatus according to claim 20, wherein the transmitter completes a transmission of the data even when a response for the transmitted data is returned from the receiver, once the transmitter has started to re-transmit the data stored in the buffer.

23.   (Previously presented)   The apparatus according to claim 20, wherein the transmitter and the receiver have the same configuration.

24.   (Previously presented)   The apparatus according to claim 20, wherein the transmitter and the receiver have respective configuration registers.

25.   (Previously presented)   An apparatus comprising:

a transmitter that serially transmits data with a predetermined size to a receiver, the data having an identifier number and an error check data, the transmitter repeatedly transmitting the data without waiting for a response from the receiver;

an error detector, coupled to the transmitter, which detects a link error when the transmitted data is not received by the receiver;

a process unit that sets the transmitter to an error recovery state when the link error is detected; and

a buffer, coupled to the transmitter, which stores the transmitted data that is not received by the receiver, and wherein the transmitter transmits first predetermined bit pattern data to the receiver when the transmitter is in the error recovery state, transmits second predetermined bit pattern data to the receiver after receiving a response of the first predetermined bit pattern data from the receiver, and transmits the data stored in the buffer when a link error is recovered.

26.   (Previously presented)   The apparatus according to claim 25, wherein the receiver detects a discontinuity of the identifier numbers of data received.

27.   (Previously presented)   The apparatus according to claim 25, wherein the receiver transmits a negative acknowledgement to the transmitter when a receiving buffer is overflowed.

28.   (Previously presented)   The apparatus according to claim 25, wherein the receiver transmits a negative acknowledgement to the transmitter when the identifier numbers of data received is discontinuous.

29.   (Currently amended)   A data transfer apparatus ~~in which data required to transmit a bus transaction is transmitted between first and second controllers that are respectively connected to first and second buses, the apparatus~~ comprising:

a first ~~transmitter~~ <u>controller</u> that transmits a predetermined number of blocks of data ~~from the first controller~~ to ~~the~~ <u>a</u> second controller without waiting for a response from the second controller, the transmitted blocks of data having consecutive identifier numbers;

a response unit that transmits from the second controller to the first controller the response when the second controller correctly receives an block of data and a re-transmission request when the second controller does not correctly receive an block of

data, the response having the identifier number of the received block of data, the re-transmission request having no identifier number;

a manager that detects an identifier number of the latest response[[;]],

wherein the first controller, a second transmitter which, when the response is received by the first controller, transmits from the first controller to the second controller a block of data having an identifier number that follows the identifier number of the latest block of data transmitted from the first transmitter[[;]], and

a third transmitter which, when the re-transmission request is received by the first controller, transmits from the first controller to the second controller a block of data having an identifier number that follows the identifier number of the latest response.

30.   (Currently amended)   The apparatus according to claim 29, wherein a configuration of the first controller is the same as a configuration of and the second controller have the same configuration.

31.   (Previously presented)   The apparatus according to claim 29, wherein the first controller and the second controller have respective configuration registers.

32.   (Previously presented)   A data transfer apparatus in which data required to transmit a bus transaction is transmitted between first and second controllers respectively connected to first and second buses, the computer system comprising:

a transmitter that repeatedly transmits a predetermined number of blocks of data from the first controller to the second controller without waiting for a response from the second controller, the transmitted blocks of data having consecutive identifier numbers;

a response unit that transmits from the second controller to the first controller the response when the second controller correctly receives a block of data, the response having the identifier number of the received block of data;

a manager that detects the identifier number of the latest response; and

a transmission controller that makes the transmitter repeatedly transmit another predetermined number of blocks of data from the first controller to the second controller without waiting for a response from the second controller, the another predetermined number of blocks of data including blocks of data having identifier numbers that follow the identifier number of the latest response.

33.   (Previously presented)   The apparatus according to claim 32, wherein the first controller and the second controller have the same configuration.

34.   (Previously presented)   The apparatus according to claim 32, wherein the first controller and the second controller have respective configuration registers.

35.   (Previously presented)   A data transfer apparatus in which data required to transmit a bus transaction is transmitted between first and second controllers respectively connected to first and second buses, the computer system comprising:

a first transmitter that transmits a predetermined number of blocks of data from the first controller to the second controller without waiting for a response from the second controller, the transmitted blocks of data having consecutive identifier numbers;

a response unit that transmits from the second controller to the first controller the response when the second controller correctly receives a block of data, the response having the identifier number of the received block of data;

an error detector that detects a link error between the first controller and the second controller when the first controller receives the responses having nonconsecutive identifier numbers;

an error recovery processing unit that repeatedly exchanges a predetermined bit pattern between the first controller and the second controller and transmits from the second controller to the first controller a re-transmission request requesting re-transmission of the blocks of data that are not correctly received by the second controller when a condition in which a serial data transfer between the first controller and the second controller is met; and

a second transmitter that re-transmits a block of data from the first controller to the second controller which is requested by the re-transmission request.

36.   (Previously presented)   The apparatus according to claim 35, wherein the first controller and the second controller have the same configuration.

37.   (Previously presented)   The apparatus according to claim 35, wherein the first controller and the second controller have respective configuration registers.